WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a field oxide film formed on a semiconductor substrate of one conductivity type;

a gate electrode formed through a gate oxide film on the semiconductor substrate of one conductivity type, which is surrounded by the field insulation film;

a low concentration source/drain region of a reverse conductivity type formed in a region surrounded by the field oxide film and the gate electrode;

an interlayer film for electrically isolating the gate electrode and the low concentration source/drain region of the reverse conductivity type from a wiring formed thereon;

a contact hole formed in the interlayer film for electrically connecting between the wiring, and the gate electrode and the low concentration source/drain region of the reverse conductivity type;

a nitride film formed for preventing the semiconductor substrate of one conductivity type from being overetched when forming the contact hole in the interlayer film; and

a high concentration diffusion layer of a reverse conductivity type selectively formed only in the low concentration source/drain region of the reverse conductivity type where the contact hole is formed.

2. A semiconductor device according to claim 1, wherein the low concentration source/drain region of the reverse conductivity type has an impurity concentration of 1×10^{16} to 1×10^{18} atoms/cm^3.

3. A semiconductor device according to claim 1, wherein the high concentration diffusion layer of the reverse conductivity type has an impurity concentration of 1×10^{19} to 5×10^{20} atoms/cm^3.

4. A semiconductor device according to claim 1, wherein the nitride film has a film thickness of 100 to 500 Å.

5. A manufacturing method for a MOS type transistor comprising:

forming a gate insulating film on a surface of a semiconductor substrate;

forming a gate electrode on the gate insulating film through patterning;

forming a low concentration diffusion region by doping an impurity into the surface of the semiconductor substrate using the gate electrode as a mask through ion implantation;

forming a nitride film over an entire surface;

forming an interlayer film containing the impurity on the entire surface of the nitride film and leveling the interlayer film through heat treatment;

selectively etching the interlayer film to form a contact hole onto the low concentration diffusion region and the gate electrode;

forming a high concentration diffusion region by doping the impurity into the surface of the semiconductor substrate using the contact hole as the mask through the ion implantation;

performing the heat treatment;

depositing a metal material into a film on the entire surface by vacuum evaporation or sputtering and patterning the metal material by photolithography or etching; and

covering the entire semiconductor substrate with a surface protective film.

6. A manufacturing method for a semiconductor device according to claim 5, wherein the interlayer film containing the impurity comprises a BPSG interlayer film.

7. A manufacturing method for a semiconductor device according to claim 5, wherein the heat treatment after the formation of the oxide film containing the impurity is carried out at 800 to 1,050°C for 3 minutes or less for activation of the impurity.